SC3-383

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10068014	02/05/2002	~~257~~ 438	382	~~2826~~ 2812	Mandala

**APPLICANTS: Joyner Keith; Rodder Mark;

**CONTINUING DATA VERIFIED:

THIS APPLN CLAIMS BENEFIT OF 60/266,899 02/06/2001

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		TI-29912
Verified and Acknowledged Examiners's intials			

TITLE : Method for manufacturing and structure for transistors with reduced gate to contact spacing

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	Application Examiner
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE		

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